



## Description

### JMT P-channel Enhancement Mode Power MOSFET

#### Features

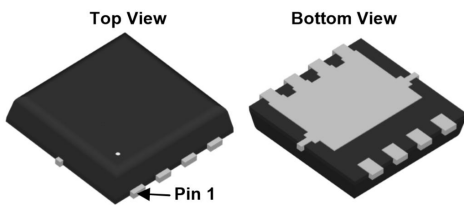
- $V_{DS}=-20V$ ,  $I_D=-55A$   
 $R_{DS(ON)} < 8.3m\Omega$  @  $V_{GS} = -4.5V$   
 $R_{DS(ON)} < 10.4m\Omega$  @  $V_{GS} = -2.5V$
- High Power and Current Handling Capability
- Lead Free Product is Acquired
- Surface Mount Package

#### Application

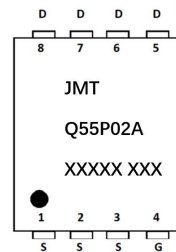
- PWM Applications
- Load Switch



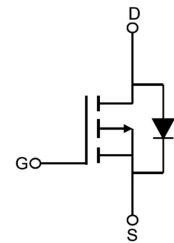
*100% UIS TESTED!*  
*100% ΔVds TESTED!*



PDFN3x3-8L



Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
JMTQ55P02A	JMTQ55P02A	TAPING	PDFN3x3-8L	13inch	5000	50000

## Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current	$T_C = 25^\circ C$	-55
		$T_C = 100^\circ C$	-35
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	-220	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note2</sup>	90	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ C$	66
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.9	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> = -250μA	-20	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V,	-	-	-1	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±12V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-0.4	-0.65	-1.0	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance <small>note3</small>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-15A	-	6.6	8.3	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-12A	-	8	10.4	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f = 1.0MHz	-	4770	-	pF
C <sub>oss</sub>	Output Capacitance		-	570	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	502	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-10V, I <sub>D</sub> =-15A, V <sub>GS</sub> =-4.5V	-	56	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	8	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	16	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =-10V, I <sub>D</sub> =-13A, R <sub>GEN</sub> =2.7Ω, V <sub>GS</sub> =-10V	-	11	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	110	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	157	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	160	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	-55	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-220	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> =-30A	-	-	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	T <sub>J</sub> =25°C, I <sub>S</sub> =-15A,	-	23	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=-100A/μs	-	14	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

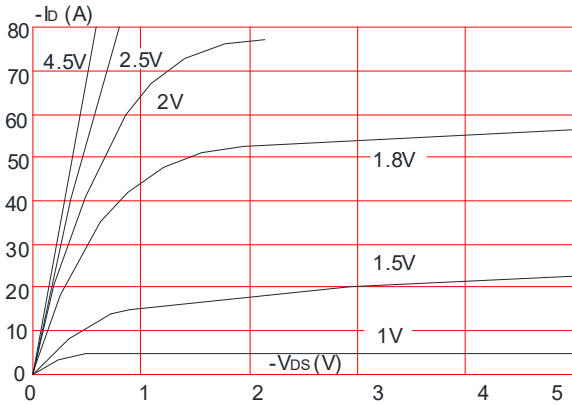
2. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=-10V, V<sub>G</sub>=-10V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=-19A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

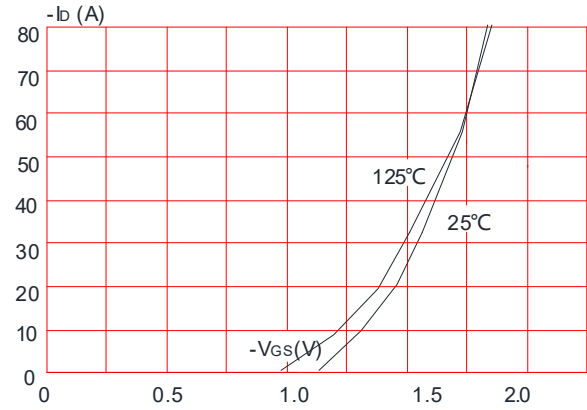


## Typical Performance Characteristics

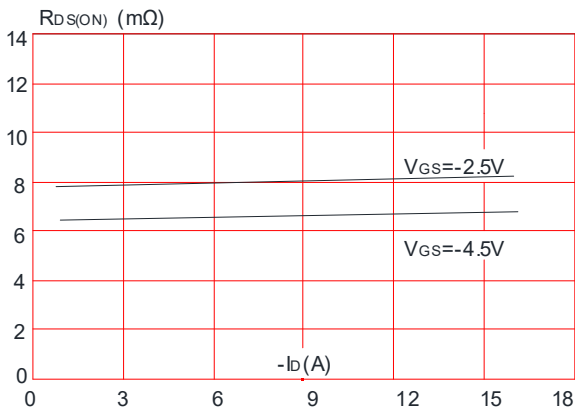
**Figure 1:** Output Characteristics



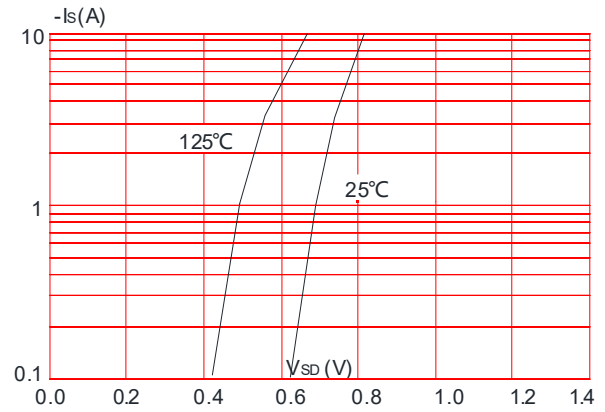
**Figure 2:** Typical Transfer Characteristics



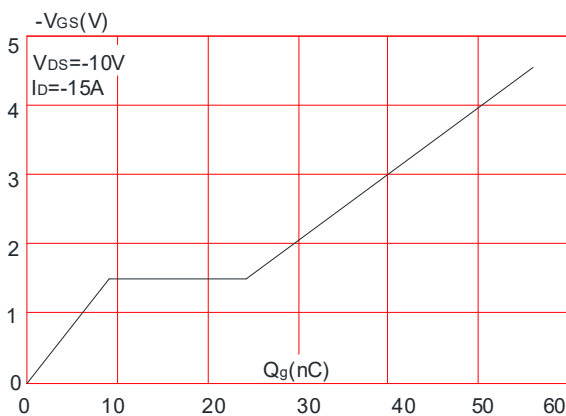
**Figure 3:** On-resistance vs. Drain Current



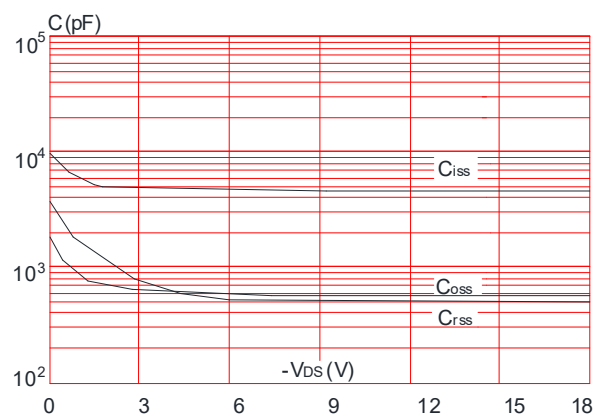
**Figure 4:** Body Diode Characteristics



**Figure 5:** Gate Charge Characteristics

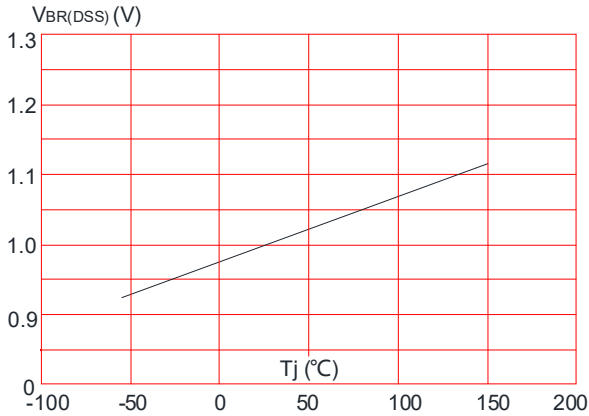


**Figure 6:** Capacitance Characteristics

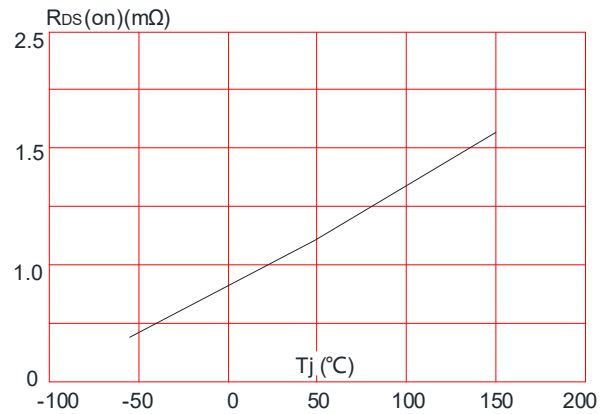




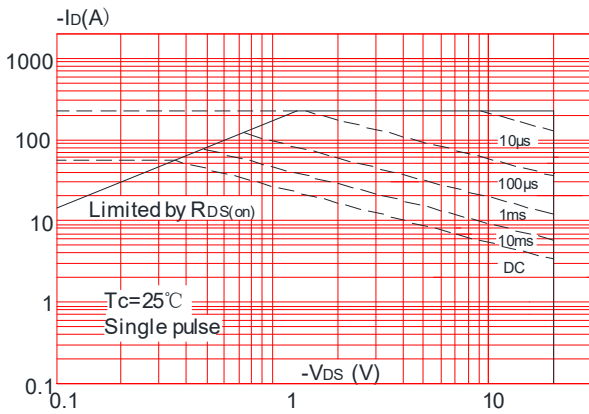
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



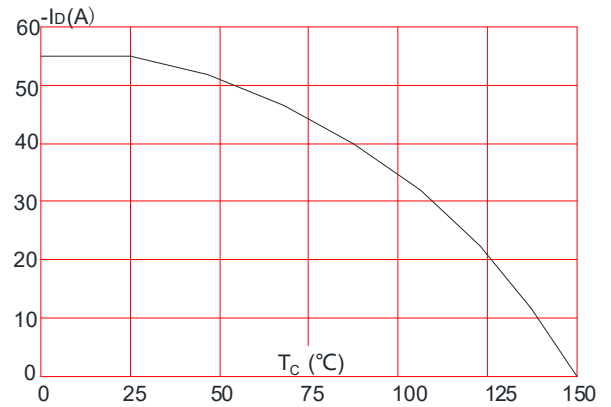
**Figure 8:** Normalized on Resistance vs. Junction Temperature



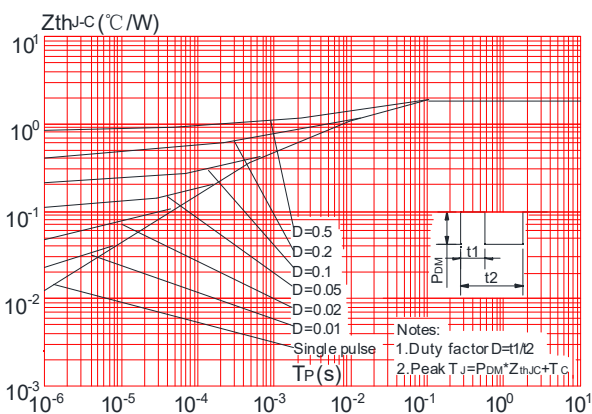
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature

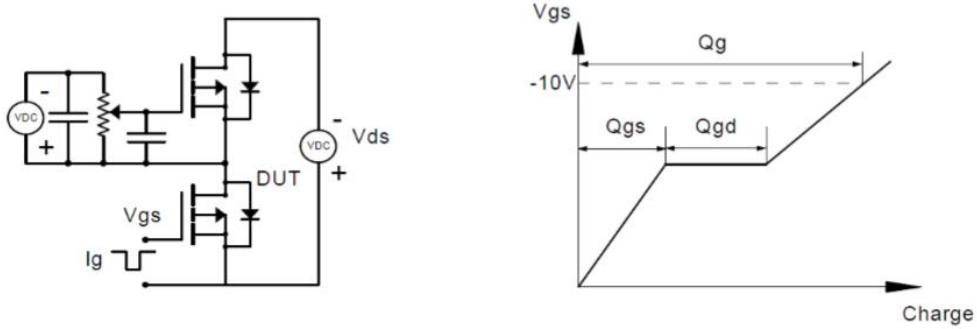


**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case

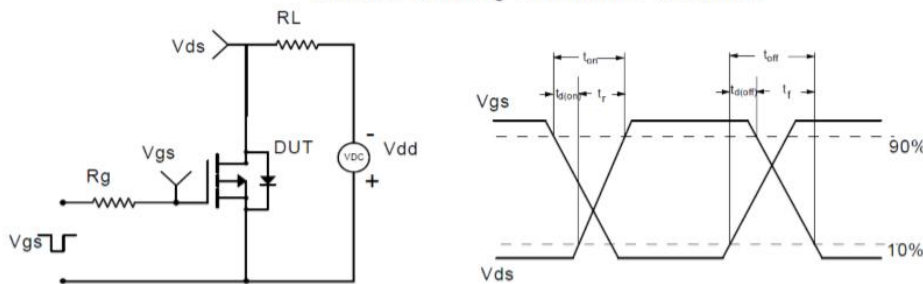


## Test Circuit

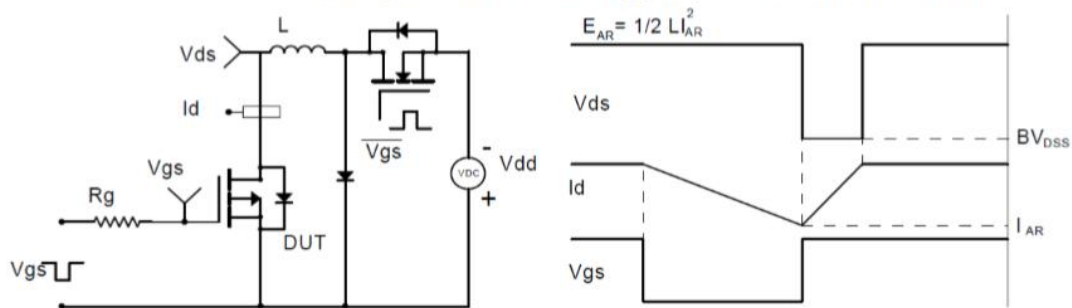
### Gate Charge Test Circuit & Waveform



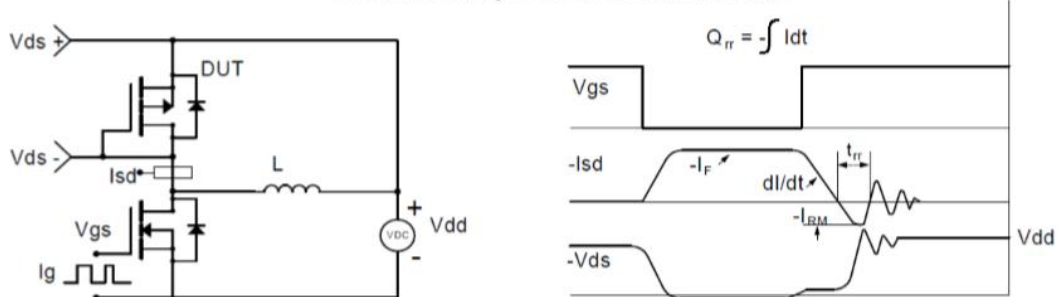
### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

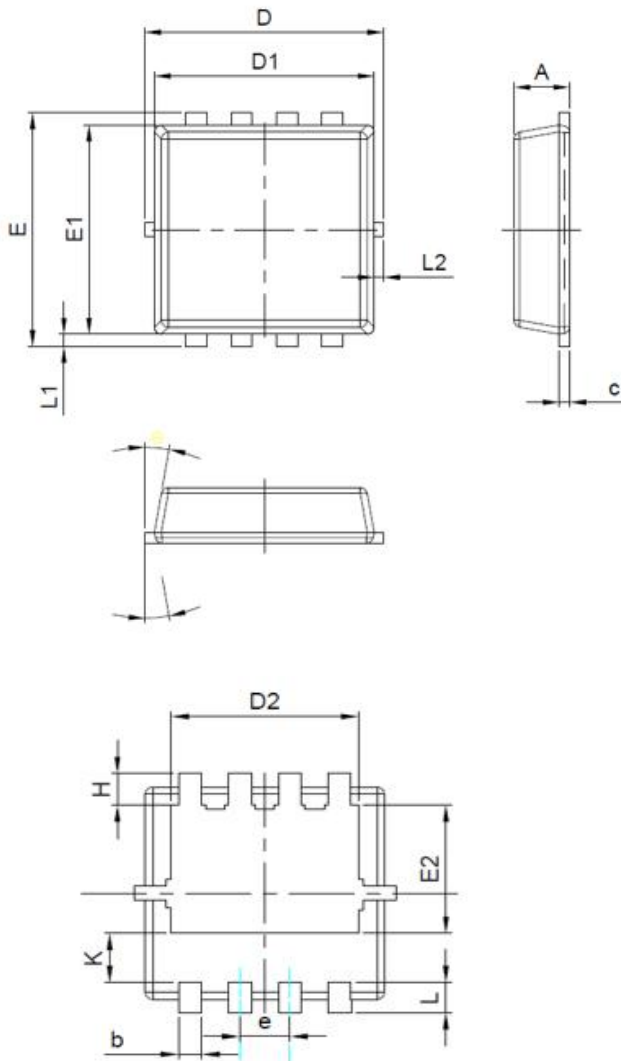


### Diode Recovery Test Circuit & Waveforms





## Package Mechanical Data-PDFN3x3-8L



COMMON DIMENSIONS  
( UNITS OF MEASURE = MILLIMETER )

SYMBOL	MIN	NOM	MAX
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.25
D	3.20	3.30	3.40
D1	3.00	3.15	3.30
D2	2.35	2.45	2.55
e	0.65 BSC		
E	3.25	3.35	3.45
E1	2.85	3.00	3.15
E2	1.635	1.735	1.835
H	0.33	0.48	0.63
K	0.585	0.685	0.785
L	0.30	0.40	0.50
L1	0.05	0.15	0.25
L2	-	-	0.15
∅	8°	10°	12°

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